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ACCELERATED SEISMIC IMAGING

Starbridge has teamed with TRICON Geophysics, Inc. and Essential Seismic Solutions to dramatically increase the speed and reduce the cost of seismic imaging.

Current methods to increase processing throughput depend mainly on creating large computing clusters. This approach incurs high electrical and air conditioning costs, requires a large administration staff, takes up ever-increasing amounts of space, and ultimately provides a diminishing return on investment as clusters grow larger.

Starbridge Hypercomputers® reduce the cost of seismic imaging and significantly speed up the process. Hypercomputing uses FPGAs to reduce the time required to perform highly compute-intensive algorithms. Starbridge is the only company working with Seismic partners to apply massively parallel, linearly scalable FPGA based Hypercomputers to greatly accelerate seismic data processing at a fraction of current costs.

Hypercomputers can accelerate TRICON's Tsunami Imaging Suite, which implements the Kirchhoff prestack time and depth migration algorithms. The Tsunami Imaging Suite, which runs on Linux clusters , images data up to seven times faster than other widely used software applications. By porting the Tsunami Suite computational kernel to a Starbridge Hypercomputer, it is anticipated to deliver over 100 times the current performance, thus replacing hundreds, or even thousands, of cluster nodes, and delivering the jobs *much* faster.

» Learn more about the Tsunami Suite

» Learn more about Hypercomputers

Field-Programmable Custom Computing Machines, 12th Annual IEEE Symposium on (FCCM'04)
April 20 - 23, 2004
Napa, California

pp. 207-216 • **Accelerating Seismic Migration Using FPGA-Based Coprocessor Platform**

Chuan He, Mi Lu, Chuanwen Sun, **Texas A&M University, College Station, TX**

Migration is the most important seismic data processing method that recovers subsurface images of the Earth's interior using surface-recorded data volumes obtained from seismic reflection surveys. A reconfigurable coprocessor platform called SPACE (Seismic data Processing Accelerator with reConfigurable Engine) using Field Programmable Gate Array (FPGA) technology is proposed in this paper to speed up these computationally demanding and data-intensive seismic migration applications. The proposed SPACE platform is characterized by its simple architecture and abundant on-board memory resources along with ultra-wide memory bandwidth, which also makes the platform suitable for other seismic data processing methods or some large-scale scientific computing applications. The time-consuming kernel part of the Pre-Stack Kirchhoff Time Migration (PSTM) algorithm is programmed into the FPGA-based coprocessor platform, which acts as a hardware accelerator attached to an Intel-based workstation through the local Peripheral Controller Interface (PCI) bus. Improved performance can be achieved by integrating a number of parallel running fully pipelined arithmetic modules into a single FPGA chip. Our simulation results show that the proposed coprocessor platform operating at a conservative speed of 50 MHz can calculate the Kirchhoff summations for 50 million points per second, which is about 15.6 times faster than a referential 2.4 GHz Pentium 4 workstation. The impressive performance of the proposed platform implies its broad applications in seismic data processing industry.

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New FPGA-based PowerRACE-e Performs Image Processing Functions 10-15x Faster than PowerPC

FFT, Pulse Compression, Image Processing Handled on PMC; Carriers Dramatically Reduces Processor Board Count and System Size

Long Beach, CA (PRWEB) January 19 2004--TEK Microsystems, Inc. of Chelmsford MA today announced the PowerRACE™-3, the first platform to combine high density FPGAs, onboard switched fabric, PowerPCs, and PMC interfaces. In this new breed of embedded platform, high speed I/O and image processing are done in a single slot. For example, in a complex image processing application such as UAVs (unmanned aerial vehicles) or in advanced industrial inspection, the PowerRACE-3 can reduce system board count by up to 40 percent, reducing weight, power, volume and cost.

This is the first platform to fully utilize the high gate density (3 million gates) and on chip processors featured in devices such as the VirtexII Pro from Xilinx. TEK Microsystems PowerRACE-3 boards and systems combine PowerPC and FPGA processing engines with powerful PMC I/O capabilities.

"The announcement of the PowerRACE-3 is TEK Microsystems' next step toward providing complete embedded systems," said Andy Reddig, president and CTO of TEK Microsystems. "As the leader in both high performance PMC I/O modules and integrated I/O solutions for switched fabrics, we have been continually enhancing our technology to handle a larger and larger part of the embedded computing challenge. It's the new embedded paradigm -- using FPGAs and flexible, core-based switched fabrics. The PowerRACE-3 is the first tightly integrated PowerPC-based platform to deliver customizable I/O with the convenience of built-in intelligent stream management. As a client-server solution, it includes a common API that provides rapid technology insertion with low integration risk and a seamless migration path."

The PowerRACE-3 uses two 533 MHz 440GX PowerPC processors to support high throughput without incurring host processor overhead. Currently supporting the RACE++ interconnect fabric, future implementations will be fabric agnostic. An on-board fabric allows each PMC site to transfer data concurrently to off-board RACE++ ports, FPGA processing or to memory thereby eliminating fabric contention and maximizing overall system performance. Configured with any one of the more than 30 available TEK Microsystems PMC modules, the new PowerRACE-3 delivers unmatched speed and flexibility.

Included with the PowerRACE-3 is the tekX software environment, providing tools for fabric configuration, buffer management, data transfer, interprocessor communications, data storage/playback and integration of streaming FPGA and I/O modules. tekX reduces system development cycles by using a common API to shield the developer from the complexities of the fabrics and the hardware. The tekX environment supports all current PowerRACE models and will support integration of future products without application changes. The result is low integration risk and seamless technology upgrades.

PMC/XMC Modules
The PowerRACE-3 can be configured with any of the more than 30 TEK Microsystems PMC I/O modules. TEK PMC modules are built as two separate pieces. The front end interfaces for FPDP, HOTLink I and II, Channel Link, LVDS, TAXI, and more, are married to one of three standard back end interfaces for 32-bit and 64-bit PCI. The back end interfaces all use FPGAs so that customer specific code can be easily downloaded for maximum flexibility, throughput and performance. Using this design methodology TEK brings the latest technologies to market as they emerge. XMC modules are currently under development.

The PowerRACE-3 is available 10-12 weeks ARO and is priced beginning at $17,500.

Photos are available: Contact Dianne McDermott e-mail protected from spam bots

TEK Microsystems, Inc., founded in 1981 and headquartered in Chelmsford Massachusetts, designs, manufactures and markets a wide range of advanced high-performance boards and systems for embedded real-time computing systems. Our comprehensive product line includes PowerRACE carrier boards based on the RACEway standard and more than 30 PMC cards (PCI Mezzanine Cards). These products are used in real-time systems designed for data acquisition, instrumentation, control systems and signal processing in customer applications such as reconnaissance, signals intelligence, satellite telemetry, mine detection, medical imaging, radar, sonar, semiconductor inspection and seismic research.

CONTACT INFORMATION

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Fpga-Based System Design - $85.44 - Wal-Mart
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FPGA Research

At the University of Toronto

University of Toronto has one of the most active FPGA research groups in the world. Comprising at least 5 faculty members and countless graduate students, we perform research in the following areas:

- FPGA Architecture
- FPGA CAD
- Reconfigurable Processors
- Field-Programmable Analog Arrays
- Synthetic Circuit Generation (2 generations of code available!)
- Automatic Circuit Design and Layout of FPGAs
- Hybrid FPGA Architectures (LUT/PLA blocks)
- Non-Uniform FPGA Routing Architectures
- VPR: Timing-Driven Packing, Placement and Routing Tool for FPGAs (code available!)
- The Transmogrifier-4 Field-Programmable System (coming soon)
- The Transmogrifier-3 Field-Programmable System
- The Transmogrifier-2 Field-Programmable System
- The Transmogrifier-1 Field-Programmable System
- The Transmogrifier C Hardware Description Language and Compiler
- SEGA: A Detailed FPGA Router
- FPGA Families
- OneChip: An FPGA processor with reconfigurable logic

Upcoming and recent conferences in FPGAs, CAD, and VLSI

Back to EECG home page

FPGA Architecture Research - Jonathan Rose

Each basic *tile* of an FPGA now consists of several thousand transistors. It is appropriate to think of the high-level design of this unit as an *architectural* problem, as this high level organization can take on many different forms. The major architectural issues are:

1. **Basic Logic Block Architecture** - the combinational and sequential functions of the logic block. Should the logic block be a two input NAND gate? NO![Rose90] It should usualy be something more coarse grained (bigger) because FPGA wires are expensive and slow, and so hooking up many small logic functions results in expensive and slow programmable logic. We have recently revisited this question, using much more modern CAD tools, architectural exploration methodologies and circuit modelling. While the original conclusions have not dramatically changed, some of the more favoured blocks are different, and the reasons for their superiority have changed. See [Ahmed00], as well as Elias Ahmed's Master's Thesis.

2. **Memory** has always been important in digital circuits, and we have looked at including memory inside FPGAs in a number of ways. First, as a standalone centralized memory: In [Wilton95], we studied the architecture of standalone memory and in [Ngai95], we built one. After that we looked at various aspects of the interconnection between distributed memory blocks in a programmable logic fabric: [Wilton96], [Wilton99], and [Wilton01].

3. **Cluster**-based logic block architecture, in which several such basic logic elements are grouped into "fully-connected" groups have become important in recent years. We can show that certains sizes of clusters have superior area [Betz96] [Betz98] and performance [Marq99], as well as [Ahmed00].

4. **Basic Routing Architecture** - the manner in which wires programmable switches are placed between the logic in order to make the programmable connections. At the beginning of research in this area, it was a not very well understood issue. The publications [Rose90] and [Rose91] were among the first to ask and answer the basic questions and create the basic terminology.

5. **The Global Routing Architecture** dictates the quantity of wires present in "big" picture manner on the chip. For example, the global routing architecture could be that there are more tracks per channel on the periperhy of the chip than in the core, or vice-verse. It could also say that there are more horiztonal wires than vertical per channel. The work in [Betz96] and [Betz96] describes the advantages (and suprising lack thereof) many possible global routing architectures.

6. **The Detailed Routing Architecture** of FPGAs has an strong effect on the speed performance of FPGAs, particularly as they are fabricated in deep-submicron processes. In particular the need for active buffers in the routing is now clear. However, buffers are not always needed, and so a key question is what proportion of the (necessarily prefabricated) routing resources should contain buffers? A related question is how long should the prefabricated wires be? This and many other questions are addressed in the book **Architecture and CAD for Deep-Submicron FPGAs**. A local description of the book can be found here . Also, a shorter version of some of the routing issues can be found in [Betz99a]. The paper [Betz99b] describes the electrical design necessary to realize these gains. The Altera Stratix routing architecture, described in [Lewis03] takes routing architecture several steps further, with a fully buffered architecture.

   We have also looked at issues dealing with the mixture of buffers and pass transistors in programmable routing [Sheng01] and issues dealing with nearest neighbour connectivity between logic blocks in an FPGA [Roopchansingh02].

➢ Research on FPGAs at the University of Toronto.

➢Return to Jonathan Rose's Page .➢Computer Group.

FPGA

Last modified: Tuesday, May 13, 2003

Short for *Field-Programmable Gate Array,* a type of logic chip that can be programmed. An FPGA is similar to a PLD, but whereas PLDs are generally limited to hundreds of gates, FPGAs support thousands of gates. They are especially popular for prototyping integrated circuit designs. Once the design is set, hardwired chips are produced for faster performance.

•E-mail this definition to a colleague•

*For internet.com pages about **FPGA** CLICK HERE. Also check out the following links!*

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FPGA links page
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integrated circuit

PLD

research institutions, educational projects, non-profit organizations, tutorials, and consultants.

FPGA Research

Home page for the FPGA research group at the University of Toronto. Includes links to special FPGA research areas as well as related resources.

List of FPGA-based computing machines

Contains a n alphabetical list of FPGA-based computing machines. Each entry provides technical details and contact information.

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	5	amorphous$3 same comput$7 same system$3 and fpga	US-PGPUB; USPAT	OR	ON	2005/01/31 13:12
L2	11	amorphous$3 same comput$7 same system$3 and (fpga or (field same programmable same gate same array))	US-PGPUB; USPAT	OR	ON	2005/01/31 13:13
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L15	26	("4286319" "4351025" "4414624" "4816993" "5025369" "5198979" "5307496" "5361373" "5404296" "5428783" "5430734" "5537319" "5550787" "5600845" "5657223" "5734829" "5944779" "5991695" "5995904" "6049759" "6061730" "6112225" "6115764" "6134599" "6304916" "6330583" "6446007" "6496969" 2003/0023576 2003/0028590 2003/0028590 "6535940" 2003/0115096).pn. and compute$4	US-PGPUB; USPAT	OR	ON	2005/01/31 16:17
L16	5	("4286319" "4351025" "4414624" "4816993" "5025369" "5198979" "5307496" "5361373" "5404296" "5428783" "5430734" "5537319" "5550787" "5600845" "5657223" "5734829" "5944779" "5991695" "5995904" "6049759" "6061730" "6112225" "6115764" "6134599" "6304916" "6330583" "6446007" "6496969" 2003/0023576 2003/0028590 2003/0028590 "6535940" 2003/0115096).pn. and compute$4 and fpga	US-PGPUB; USPAT	OR	ON	2005/01/31 16:17
L17	5	("4286319" "4351025" "4414624" "4816993" "5025369" "5198979" "5307496" "5361373" "5404296" "5428783" "5430734" "5537319" "5550787" "5600845" "5657223" "5734829" "5944779" "5991695" "5995904" "6049759" "6061730" "6112225" "6115764" "6134599" "6304916" "6330583" "6446007" "6496969" 2003/0023576 2003/0028590 2003/0028590 "6535940" 2003/0115096).pn. and compute$4 and (fpga or (programmable same gate same array))	US-PGPUB; USPAT	OR	ON	2005/01/31 16:18

L18	0	("4286319" "4351025" "4414624" "4816993" "5025369" "5198979" "5307496" "5361373" "5404296" "5428783" "5430734" "5537319" "5550787" "5600845" "5657223" "5734829" "5944779" "5991695" "5995904" "6049759" "6061730" "6112225" "6115764" "6134599" "6304916" "6330583" "6446007" "6496969" 2003/0023576 2003/0028590 2003/0028590 "6535940" 2003/0115096).pn. and compute$4 and (fpga or (programmable same gate same array)) and kirchoff	US-PGPUB; USPAT	OR	ON	2005/01/31 16:19
L19	0	("4286319" "4351025" "4414624" "4816993" "5025369" "5198979" "5307496" "5361373" "5404296" "5428783" "5430734" "5537319" "5550787" "5600845" "5657223" "5734829" "5944779" "5991695" "5995904" "6049759" "6061730" "6112225" "6115764" "6134599" "6304916" "6330583" "6446007" "6496969" 2003/0023576 2003/0028590 2003/0028590 "6535940" 2003/0115096).pn. and compute$4 and (fpga or (programmable same gate same array)) and seismic	US-PGPUB; USPAT	OR	ON	2005/01/31 16:19
L20	5	("4286319" "4351025" "4414624" "4816993" "5025369" "5198979" "5307496" "5361373" "5404296" "5428783" "5430734" "5537319" "5550787" "5600845" "5657223" "5734829" "5944779" "5991695" "5995904" "6049759" "6061730" "6112225" "6115764" "6134599" "6304916" "6330583" "6446007" "6496969" 2003/0023576 2003/0028590 2003/0028590 "6535940" 2003/0115096).pn. and compute$4 and (fpga or (programmable same gate same array))	US-PGPUB; USPAT	OR	ON	2005/01/31 16:22

L21	1	("4286319" "4351025" "4414624" "4816993" "5025369" "5198979" "5307496" "5361373" "5404296" "5428783" "5430734" "5537319" "5550787" "5600845" "5657223" "5734829" "5944779" "5991695" "5995904" "6049759" "6061730" "6112225" "6115764" "6134599" "6304916" "6330583" "6446007" "6496969" 2003/0023576 2003/0028590 2003/0028590 "6535940" 2003/0115096).pn. and compute$4 and (fpga or (programmable same gate same array)) and (nodular or node$3)	US-PGPUB; USPAT	OR	ON	2005/01/31 16:19
S1	0	amorphous same comput$7 same process$3 and (geophysical or seismic) same image$3	US-PGPUB; USPAT	OR	ON	2005/01/31 13:11
S2	325	amorphous same comput$7 same process$3	US-PGPUB; USPAT	OR	ON	2005/01/18 18:25
S3	0	amorphous same comput$7 same process$3 and (geophysical or seismic)	US-PGPUB; USPAT	OR	ON	2005/01/18 15:41
S4	23	(amorphous or shapeless or fuzzy) same comput$7 same process$3 and (geophysical or seismic)	US-PGPUB; USPAT	OR	ON	2005/01/18 18:25
S5	17	(amorphous or shapeless or fuzzy) same comput$7 same process$3 and (seismic)	US-PGPUB; USPAT	OR	ON	2005/01/18 18:26
S6	0	amorphous same comput$7 same process$3 same seismic	US-PGPUB; USPAT	OR	ON	2005/01/18 18:26
S7	0	amorphous same comput$7 same process$3 and seismic	US-PGPUB; USPAT	OR	ON	2005/01/18 18:26
S8	3	(amorphous or shapeless or fuzzy) same comput$7 same process$3 same (seismic)	US-PGPUB; USPAT	OR	ON	2005/01/18 18:28
S9	35	(amorphous or shapeless or fuzzy) same comput$7 and process$3 and (seismic)	US-PGPUB; USPAT	OR	ON	2005/01/18 18:28
S10	135	(amorphous or shapeless or fuzzy) and comput$7 and process$3 and (seismic)	US-PGPUB; USPAT	OR	ON	2005/01/18 18:29
S11	135	(amorphous or fuzzy) and comput$7 and process$3 and (seismic)	US-PGPUB; USPAT	OR	ON	2005/01/18 18:29
S12	35	(amorphous) and comput$7 and process$3 and (seismic)	US-PGPUB; USPAT	OR	ON	2005/01/18 18:31
S13	4	(amorphous) same comput$7 and process$3 and (seismic)	US-PGPUB; USPAT	OR	ON	2005/01/18 18:29

S14	35	(amorphous) and comput$7 and process$3 and (seismic)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/01/18 18:31